REMARKS/ARGUMENTS

The Office Action mailed May 9, 2003, has been received and reviewed. Claims 1 through 26 are currently pending in the application. Claims 18 through 26 are allowed. Claims 1 through 17 stand rejected. Applicants have amended claims 1, 7, and 8, and respectfully request reconsideration of the application as amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,089,878 to Lee and U.S. Patent No. 5,012,323 to Farnworth

Claims 1 through 6, 9, and 13 through 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lee (U.S. Patent No. 5,089,878) and Farnworth (U.S. Patent No. 5,012,323). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Turning to the references cited in the instant rejection, Lee discloses a low impedance integrated circuit package. The integrated circuit package comprises a circuit chip 2 disposed on a support paddle 10 of a lead frame 8 (Figs. 1a-1c). Lead frame 8 is depicted as having a number of leads extending from the four sides of support paddle 10, including ground leads 12a and power leads 12b (col. 3, lines 23-30). A dielectric layer 16 is provided above the leads, and a plurality of trapezoidal metal coupons 18a and 18b are positioned over dielectric layer 16 to

provide low impedance paths for ground leads 12a and power leads 12b, respectively (col. 3, lines 36-51). Coupons 18a and 18b are connected to leads 12a and 12b via wirebonds or other conductive elements (Fig. 1c). Coupons 18a and 18b are separated from one another by decoupling capacitors 28 (Fig. 1a and col. 4, lines 5-13).

Farnworth teaches a double die semiconductor package having a back bonded die and a face bonded die interconnected on a single lead frame. In the background of the invention, Farnworth discusses prior art lead frame systems which overcome the constraints of a standard lead frame having a die bonding paddle (col. 1, line 62 - col. 2, line 38). In the first system, a die is back bonded to extensions of the individual lead frame leads (col. 2, lines 18-24). In the second system, a die is face bonded to the leads of the lead frame (col. 2, lines 24-32). Farnworth further describes two lead frame layouts for these systems: the first comprising a dual row, inline-lead embodiment, and the second comprising a single row inline-lead embodiment (Figs. 2 and 3 and col. 2, line 39 - col. 3, line 47).

Applicants respectfully submit that Lee and Farnworth, either alone or in combination, fail to teach or suggest all of the claim limitations of the presently amended claim 1.

As amended herein, claim 1 recites the limitations of a first voltage reference plane "having a portion positioned *between* a surface of said semiconductor die and said first group of lead fingers," and a second voltage reference plane "having a portion positioned *between* said surface of said semiconductor die and said second group of lead fingers." (Emphasis added.) These limitations are supported in the specification, as filed, at page 7, paragraph [0022]. The combination of Lee and Farnworth does not disclose these limitations. Rather, the coupons 18a, 18b, 38a, and 38b of Lee are depicted and described as being located above dielectric layer 16, 36 and leads 12, 30 at locations that are remote from the surfaces of integrated circuit chip 2. (Lee at Figs. 1a-1c, 3a-3b and 9-9d.) Therefore, no portions of coupons 18a, 18b, 38a, and 38b as disclosed by Lee are positioned between a surface of chip 2 and leads 12, 30. The combination of Lee with Farnworth does not overcome the failure of Lee to disclose these limitations, as the groups of lead fingers 23 BRO and 23 BLO of Farnworth are also remote from any die surface.

(Farnworth at Fig. 4.) Accordingly, claim 1 is allowable over the combination of Lee and Farnworth under the provisions of 35 U.S.C. § 103(a).

Claims 2 through 6, 9, and 13 through 17 are also allowable as depending from claim 1. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Obviousness Rejection Based on U.S. Patent No. 5,089,878 to Lee and U.S. Patent No. 5,150,194 to Brooks et al.

Claims 1 through 9 and 13 through 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lee (U.S. Patent No. 5,089,878) and Brooks et al. (U.S. Patent No. 5,150,194). Applicants respectfully traverse this rejection, as hereinafter set forth.

As discussed above, amended claim 1 recites the limitations of a first voltage reference plane "having a portion positioned *between* a surface of said semiconductor die and said first group of lead fingers," and a second voltage reference plane "having a portion positioned *between* said surface of said semiconductor die and said second group of lead fingers." (Emphasis added.) Lee discloses a low impedance integrated circuit package wherein coupons 18a, 18b, 38a, and 38b are depicted and described as being located above dielectric layer 16, 36 and leads 12, 30 at locations that are remote from the surfaces of integrated circuit chip 2. (Lee at Figs. 1a-1c, 3a-3b and 9-9d.) Therefore, no portions of coupons 18a, 18b, 38a, and 38b as disclosed by Lee are positioned between a surface of chip 2 and leads 12, 30.

Brooks et al. is directed to a integrated circuit lead frame wherein a conventional die attach paddle 11 is supported by a plurality of tie bars 16 attached to a support beam 17 that reduces bowing (Fig. 3 and Abstract). The combination of Lee with Brooks et al. also does not overcome the failure of Lee to disclose the above limitations of claim 1, as the groups of lead fingers 15 extending from the sides of die paddle 11 in Brooks et al. would also be remote from any die surface. (Brooks et al. at Fig. 3.) Accordingly, claim 1 is allowable over the combination of Lee and Brooks et al. under the provisions of 35 U.S.C. § 103(a).

Claims 2 through 9 and 13 through 17 are also allowable as depending from claim 1. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Obviousness Rejection Based on U.S. Patent No. 5,089,878 to Lee and U.S. Patent No. 5,012,323 to Farnworth, and Further in Combination with U.S. Patent No. 5,583,377 to Higgins

Claims 10 through 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lee (U.S. Patent No. 5,089,878) and Farnworth (U.S. Patent No. 5,012,323), as applied to claims 1 through 6, 9, and 13 through 17, supra, and further in combination with Higgins (U.S. Patent No. 5,583,377). Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 10 through 12 depend from claim 1. Claim 1 recites the limitations of a first voltage reference plane "having a portion positioned *between* a surface of said semiconductor die and said first group of lead fingers," and a second voltage reference plane "having a portion positioned *between* said surface of said semiconductor die and said second group of lead fingers." (Emphasis added.) As previously discussed, the combination of Lee and Farnworth does not disclose these limitations. Claims 10 through 12, which incorporate the limitations of claim 1, are accordingly allowable over Lee and Farnworth. Higgins, which is directed to a pad array semiconductor device having a heat sink with die receiving cavity, also does not teach or suggest the above described limitations of claim 1.

Applicants further submit there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings as presented in the instant application. Higgins et al. discloses a heat sink 48 which is combined with Lee and Farnworth to provide the limitations of the reference plane projections recited in claims 10, 11 and 12. All of the heat sinks disclosed by Higgins et al. are intended to be of a size sufficient to provide a die receiving cavity for holding a semiconductor die (col. 2, lines 17-23). The coupons 18a and 18b of Lee, on the other hand, are described as comprising a "thin metal foil" (col. 6, lines 37-40). Due to the significant

structural and functional differences between the heat sink 48 of Higgins et al. and the coupons 18a and 18b of Lee, it would not be obvious to combine the two to achieve the structural features recited in claims 10 through 12 of Applicants' invention. Applicants respectfully submit that this fact is born out by the comparison of the clear structural differences between the heat sink of Higgins et al. and the metal coupons of Lee, and does not amount to mere conjecture unsupported by a showing of facts, as asserted by the Office in the present Office Action. Rather, Applicants respectfully submit that the Office has impermissibly relied on the hindsight benefit of Applicants' own disclosure to construct the claimed invention. *See, e.g., Grain Processing Corp. v. American-Maize Prods. Co.,* 5 U.S.P.Q.2d 1788, 1792 (Fed. Cir. 1988).

In view of the above, Applicants respectfully submit that claims 10 through 12 are allowable over Lee, Farnworth and Higgins et al. and request the withdrawal of the rejections of these claims under 35 U.S.C. § 103(a).

Obviousness Rejection Based on U.S. Patent No. 5,089,878 to Lee and U.S. Patent No. 5,150,194 to Brooks et al., and Further in Combination with U.S. Patent No. 5,583,377 to Higgins

Claims 10 through 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lee (U.S. Patent No. 5,089,878) and Brooks et al. (U.S. Patent No. 5,150,194), as applied to claims 1 through 9 and 13 through 17, and further in combination with Higgins (U.S. Patent No. 5,583,377). Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 10 through 12 depend from claim 1. Claim 1 recites the limitations of a first voltage reference plane "having a portion positioned *between* a surface of said semiconductor die and said first group of lead fingers," and a second voltage reference plane "having a portion positioned *between* said surface of said semiconductor die and said second group of lead fingers." (Emphasis added.) As previously discussed, the combination of Lee and Brooks et al. does not disclose these limitations. Claims 10 through 12, which incorporate the limitations of claim 1, are accordingly allowable over Lee and Brooks et al. Higgins, which is directed to a pad

array semiconductor device having a heat sink with die receiving cavity, also does not teach or suggest the above described limitations of claim 1.

Applicants further submit there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings as presented in the instant application. Higgins et al. discloses a heat sink 48 which is combined with Lee and Brooks et al. to provide the limitations of the reference plane projections recited in claims 10, 11 and 12. All of the heat sinks disclosed by Higgins et al. are intended to be of a size sufficient to provide a die receiving cavity for holding a semiconductor die (col. 2, lines 17-23). The coupons 18a and 18b of Lee, on the other hand, are described as comprising a "thin metal foil" (col. 6, lines 37-40). Due to the significant structural and functional differences between the heat sink 48 of Higgins et al. and the coupons 18a and 18b of Lee, it would not be obvious to combine the two to achieve the structural features recited in claims 10 through 12 of Applicants' invention. Applicants respectfully submit that this fact is born out by the comparison of the clear structural differences between the heat sink of Higgins et al. and the metal coupons of Lee, and does not amount to mere conjecture unsupported by a showing of facts, as asserted by the Office in the present Office Action. Rather, Applicants respectfully submit that the Office has impermissibly relied on the hindsight benefit of Applicants' own disclosure to construct the claimed invention. *See, e.g., Grain Processing Corp. v. American-Maize Prods. Co.,* 5 U.S.P.Q.2d 1788, 1792 (Fed. Cir. 1988).

In view of the above, Applicants respectfully submit that claims 10 through 12 are allowable over Lee, Brooks et al. and Higgins et al. and request the withdrawal of the rejections of these claims under 35 U.S.C. § 103(a).

ENTRY OF AMENDMENTS

The amendments to claims 1, 7, and 8 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1 through 26 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

Greg T. Warder
Registration No. 50,208
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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Document in ProLaw

IN THE CLAIMS:

Claims 1, 7, and 8 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (presently amended) A semiconductor die assembly comprising:

a semiconductor die having a plurality of bond pads on an active surface thereof;

a lead frame having at least a first group of lead fingers and a second group of lead fingers to respectively extend from first and second opposing sides of said semiconductor die attached to a die-attach location on said lead frame to another, single side of said lead frame in a substantially mutually parallel configuration;

a first voltage reference plane adjacent to said first side of said semiconductor die, said first voltage reference plane ~~underlying at least~~ having a portion ~~of~~ positioned between a surface of said semiconductor die and said first group of lead fingers extending from said first side of said semiconductor die toward said another, single side of said lead frame; and

a second voltage reference plane adjacent to said second opposing side of said semiconductor die, said second voltage reference plane ~~underlying at least~~ having a portion ~~of~~ positioned between said surface of said semiconductor die and said second group of lead fingers extending from said second opposing side of said semiconductor die toward said another, single side of said lead frame.

2. (original) The assembly of claim 1, wherein said lead frame comprises a vertical surface mount package configuration.

3. (previously amended) The assembly of claim 1, wherein said first voltage reference plane and said second voltage reference plane are adhered to at least some of the lead fingers of said first group of lead fingers and said second group of lead fingers, respectively.

4. (previously amended) The assembly of claim 3, wherein said first voltage reference plane and said second voltage reference plane are adhered directly via a non-conductive adhesive to said at least some of the lead fingers of said first group of lead fingers and said second group of lead fingers, respectively.

5. (original) The assembly of claim 1, further comprising a packaging material encapsulating at least said active surface of said semiconductor die.

6. (previously amended) The assembly of claim 5, wherein said packaging material at least partially covers said first and said second voltage reference planes and said first and said second groups of lead fingers.

7. (presently amended) The assembly of claim 1, wherein said first group of lead fingers and said second group of lead fingers are attached to said semiconductor die in a lead-over-chip configuration. ~~lead frame includes a die attach paddle to which said semiconductor die is attached~~.

8. (presently amended) The assembly of claim 1, wherein said first group of lead fingers and said second group of lead fingers are attached to said semiconductor die in a lead-under-chip configuration. ~~die attach location comprises a die attach paddle~~.

9. (previously amended) The assembly of claim 1, wherein said first voltage reference plane and said second voltage reference plane are electrically connected to at least one

lead finger of said first group of lead fingers and said second group of lead fingers, respectively, which in turn is connected through a bond pad to a reference potential of said semiconductor die.

10. (previously amended) The assembly of claim 1, wherein at least one of said first voltage reference plane and said second voltage reference plane includes a plurality of projections extending outwardly from a surface of said at least one of said first voltage reference plane and said second voltage reference plane.

11. (original) The assembly of claim 10, further comprising a packaging material extending over at least one of said first voltage reference plane and said second voltage reference plane, wherein said projections extend through said packaging material.

12. (original) The assembly of claim 11, wherein said projections extend through said packaging material to an exterior surface thereof.

13. (previously amended) The assembly of claim 1, wherein said first voltage reference plane and said second voltage reference plane are of sufficient mass to measurably alter heat transfer characteristics of said assembly.

14. (original) The assembly of claim 1, further comprising a packaging material encapsulating said assembly so that only outer ends of said at least said first group of lead fingers and said second group of lead fingers extend therethrough.

15. (previously amended) The assembly of claim 1, wherein said first voltage reference plane and said second voltage reference plane extend over at least about fifty percent of a surface area of said at least said first group of lead fingers and said second group of lead fingers, respectively.

16. (previously amended) The assembly of claim 1, wherein said first voltage reference plane and said second voltage reference are separated from said at least said first group of lead fingers and said second group of lead fingers, respectively, by an insulating adhesive structure.

17. (previously amended) The assembly of claim 16, wherein said insulating adhesive structure comprises an insulating film having an adhesive on opposing surfaces thereof, one surface of said opposing surfaces being adhered to at least one of said first group of lead fingers and said second group of lead fingers and another surface of said opposing surfaces being adhered to at least one of said first voltage reference plane and said second voltage reference plane.

18. (previously three times amended) A vertical surface mount lead frame to be assembled to a semiconductor die, comprising:

a lead frame having at least a first group of lead fingers and a second group of lead fingers to respectively extend from first and second opposing sides of an intended die-attach location to another, single side of said lead frame in a substantially mutually parallel configuration;

a first voltage reference plane in immediate proximity to said first group of lead fingers and in electrical isolation therefrom, said first voltage reference plane extending across at least a turning portion of said first group of lead fingers extending from said first side of said intended die-attach location toward said another, single side of said lead frame;

a second voltage reference plane in immediate proximity to said second group of lead fingers and in electrical isolation therefrom, said second voltage reference plane extending across at least a turning portion of said second group of lead fingers extending from said second opposing side of said intended die-attach location toward said another, single side of said lead frame; and

an intervening neck extending across said another, single side of said lead frame and conductively connecting said first voltage reference plane and said second voltage reference plane.

19. (previously amended) The assembly of claim 18, wherein said first voltage reference plane and said second voltage reference plane are adhered to at least some of the lead fingers of said first group of lead fingers and said second group of lead fingers, respectively.

20. (previously amended) The assembly of claim 19, wherein said first voltage reference plane and said second voltage reference plane are adhered directly via a non-conductive adhesive to said at least some of the lead fingers of said first group of lead fingers and said second group of lead fingers, respectively.

21. (original) The assembly of claim 18, wherein said lead frame includes a die-attach paddle to which said semiconductor die is attached.

22. (original) The assembly of claim 18, wherein said die-attach location comprises a die-attach paddle.

23. (original) The assembly of claim 18, wherein at least one of said first voltage reference plane and said second voltage reference plane includes projections extending away from a direction of said immediate proximity of said first group of lead fingers and said second group of lead fingers, respectively.

24. (previously twice amended) The assembly of claim 18, wherein said first voltage reference plane and said second voltage reference plane extend across at least about fifty percent of a surface area of said at least said first group of lead fingers and said second group of lead fingers, respectively.

25. (original) The assembly of claim 18, wherein said first voltage reference plane and said second voltage reference is separated from said at least said first group of lead fingers and said second group of lead fingers, respectively, by an insulating adhesive structure.

26. (previously amended) The assembly of claim 25, wherein said insulating adhesive structure comprises an insulating film having an adhesive on opposing surfaces thereof, one surface of said opposing surfaces being adhered to at least one of said first group of lead fingers and said second group of lead fingers and another surface of said opposing surfaces being adhered to at least one of said first voltage reference plane and said second voltage reference plane.